Digital Auto-Tuning System for Analog Filters

G. Zatorre, S. Celma, C. Aldea, N. Medrano
Dpto. de Ingeniería Electrónica y Comunicaciones
Universidad de Zaragoza
Grupo de Diseño Electrónico, I3A
Zaragoza, Spain
{gzatorre, scelma, caldea, nmedrano}@unizar.es

E. Peralías
Instituto de Microelectrónica de Sevilla, IMSE. Centro Nacional de Microelectrónica, CNM
Consejo Superior de Investigaciones Científicas, CSIC
Sevilla. Spain
peralias@imse.cnm.es

***Abstract*—In this paper, a new self-tuning digital technique is reported for analog filters over VHF (very high frequency) applications, based on phase detector. By using a 0.35 µm Mixed Signal CMOS process, changes in frequency response of a 3rd-order low pass filter can be tuned with a 3% error over the designed value. This technique confirms the feasibility of the proposed scheme in analog filter applications. The system consumes less area, power and tuning time than other proposed schemes. Simulation results show the building viability in a 10 MHz low pass filter.**

I. INTRODUCTION

The continuous-time technique has been used to implement filters where high frequency at low cost of silicon and power is required, instead of the switched-capacitor or switched-current approaches [1]-[3]. The low cost CMOS technology is a good choice if the requirement of accuracy is relaxed and is the most economical solution if the whole mixed-signal system is implemented in a pure digital process. Among high speed signal processing applications, it is widely used in the IF band pass sections of RF front-end circuits and in the hard disk drive industry. These applications demand continuous-time filters with variable bandwidths over a wide range [4]. A possible solution could be to use discrete tuning for IF filters, in the same way that this technique is being used in other high frequency applications, such as IF-baseband strips [6] or read-channel filters [7].

On the other hand, we must not overlook the problems encountered on the analogue part in the current digital CMOS processes associated with the scaling down and low-voltage operation. Among these, the reduced dynamic range is of concern, making difficult conventional continuous tuning to compensate technological and temperature spreads. So, it is necessary to provide an on-chip automatic tuning scheme to achieve an accurate filter performance [8]-[9]. This circuit tunes the characteristic filter frequency in order to compensate fabrication tolerances, temperature variations and ageing. We can take advantage of the simplicity of the digital control algorithms to adjust the tunable analogue part, thus yielding a considerable saving of area and power.

In this paper, an innovative digital frequency auto-tuning technique is presented for use in integrated continuous-time filters which is simpler than other schemes [10]-[11] and which needs less silicon and power. A 4-bit digitally auto-tuned third order low-pass filter was simulated using this technique yielding a 10 MHz fixed cut-off frequency low-pass filter with an error below 3% and tuning time lower than 1.6 µs. Post-layout simulation results and Monte Carlo analysis show the implementation viability which are presented in this communication.

Section II introduces the tuning strategies to tuning continuous-time filters. Section III describes the overall system and its basic component blocks. With special emphasis, it is described the phase detector block which carries out the main operation in the new auto-tuning technique. Section IV presents the proposed phase detector deep viability study with simulation results and Monte Carlo analysis. Conclusions are given in Section V.

II. APPROACHES TO AUTO-TUNING APLICATION

Due to the analog filter characteristic parameters depends on capacitor, resistors and transconductances absolute values their CMOS integration suffers for the low resolution these technologies can provide. The variation of these elements because of the process tolerances can change the filter characteristic frequency in a 30% or even more. This issue make necessary to tune the filter characteristic parameters after the integration in order to achieve the desired precision.

The most extended strategies described in the literature to tune filters are the Master-Slave, Off-Line and Uninterrupted Off-Line approaches [12], [13] (Figure 1).

The Master-Slave approach (Figure 1a) consists on two matched sintonizable filters controlled by a tuning system. This tuning system monitors the state of the master filter and controls both filters. Due to mismatching problems, the tuning accuracy of the slave filter is limited. The Off-Line tuning approach (Figure 1b) is an attempt to overcome the

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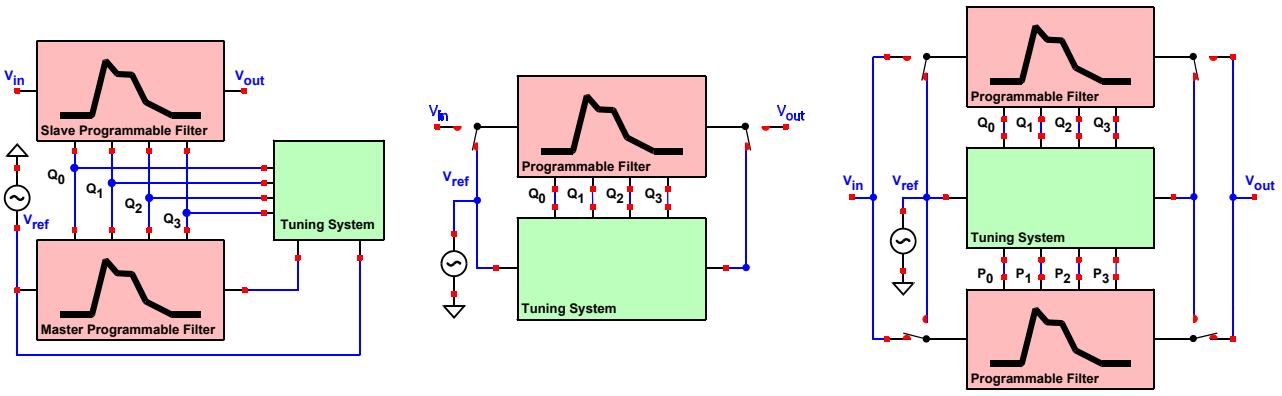

a.- Master-Slave approach b.- Off-Line approach c.- Uninterrupted Off-Line approach

Figure 1. Tuning approaches

matching problem of the Master-Slave scheme. When the signal must not be processed continuously, the system can use the off-line time to reconfigure itself. Furthermore this scheme is smaller. In the applications were the signal can not be disconnected the Uninterrupted Off-Line approach (Figure 1c) can solve the matching problem. In this approach two matched filters process the signal alternatively. In the off-line period each filter is connected to the tuning system to be re-tuned.

Of course each one of these approaches has advantages and disadvantages. The Off-Line choice is the simpler and smaller but it can not be used in all applications. Due to the Master-Slave solution suffers from the mismatching problem which limits the tuning accuracy but it is the only one scheme that provides real on-line tuning. On the other hand the Double Off-Line approach is an agreement between Master-Slave and Off-Line solutions.

The system presented in this paper can be used in all of the tuning approaches.

III. System Description

A. *Autotuning-Scheme*

The whole system is depicted in Figure 2. It consists of four blocks: an analogue filter with digitally tuneable characteristic frequency, a delayer stage, a phase detector and a double clock up/down inputs counter.

A high accuracy reference harmonic signal V_{ref} at desired filter characteristic frequency is fed into the system. This signal goes through the digitally tuneable analogue filter, yielding signal A, and into the delayer block, yielding signal B. At the desired filter output, the signal suffers a known delay which depends on the filter type and its characteristic frequency. The delayer block must provide the same delay that the desired (nominal) filter would produce in the reference harmonic signal. Only when the filter is not working at the desired characteristic frequency there is a lag between the filter and delayer outputs (A and B).

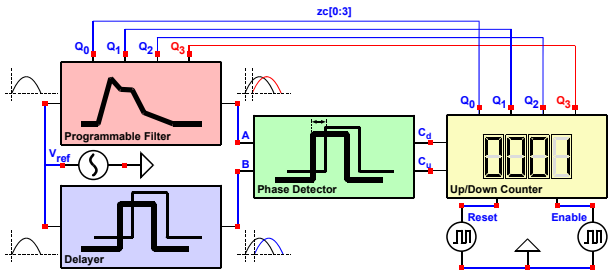

Figure 2. Overall system architecture.

The filter and delayer outputs are led into the phase detector in order to compare their relative phases. This block generates one pulse per cycle in the C_d (down) output, when the filter output signal goes ahead, and one pulse per cycle in the C_u (up) output when the filter signal is delayed. In this way, C_u and C_d signals control the up/down counter, the state of which is used to control the digitally tuneable analogue filter. When parameters such as programmability range, phase detector resolution and up/down counter bits are properly selected, the system stabilizes at the state with the filter tuned at a characteristic frequency closest to the reference signal frequency.

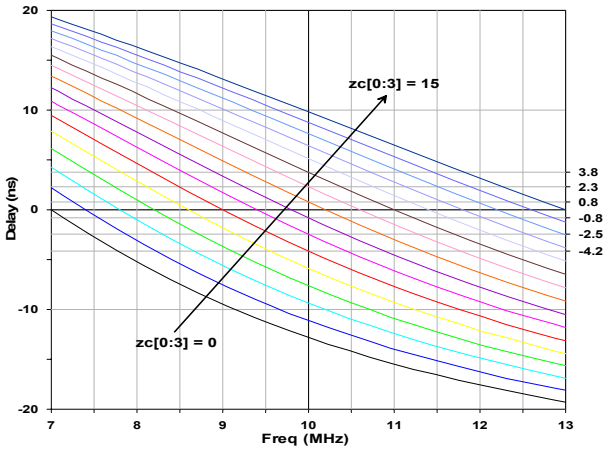

Figure 3. Tunable filter delays at nominal cut-off frequency for each programming word.

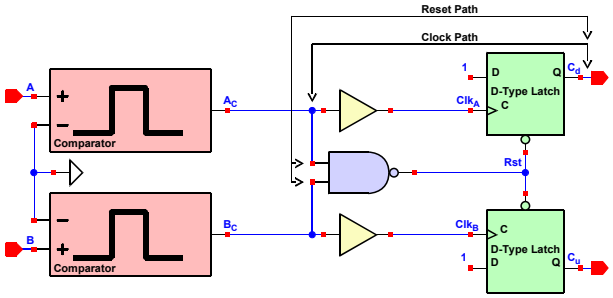

Figure 4. Phase detector scheme.

In this work, the 4-bit digitally tuneable filter was modelled using Spectre-AHDL language and reproduces the behaviour of a Butterworth third order low pass filter. Figure 3 shows the delay with regard to the signal frequency, for each *programming word* value, **zc**. As can be observed, the filter characteristic frequency can be linearly adjusted from 7 MHz to 13 MHz using the controlling 4-bit digital word. A 10 MHz characteristic frequency filter was selected in order to prove the technique viability.

The delayer block can be implemented in several ways depending on the filter phase response and characteristic frequency. To show the proposed system functionality a VerilogA-described delayer cell was used in this work.

A standard up/down binary counter with reset, enable and separate up/down clocks was used with minimal changes; a control which prevents 0 to 2^n-1 and 2^n-1 to 0 transitions was implemented. On the other hand, the more significant bit was stored in T flip-flops with reset control, while the rest of the bits where stored using T flip-flops with set control. In this way the system starts to count from 2^{n-1}-1=7 after a reset signal instead of starting from 0 or 2^n-1.

B. *Phase Detector Block Overview*

The signals to be compared, A and B, are driven through VerilogA-described identical comparators to provide digital square shape signals to the next stages, A_C and B_C as shown in Figure 4.

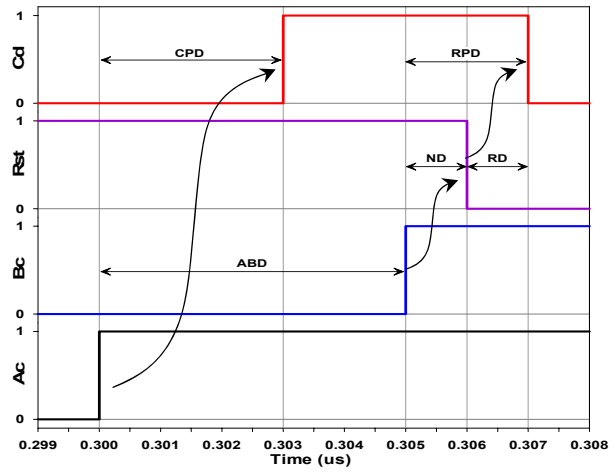

Figure 5. Phase detector delay chronograms.

These two conditioned signals are connected to the clock inputs of identical D-type flip-flops through a buffer. At the same time each of the conditioned signals is connected to each one of a NAND gate input whose output is attached to both of the flip-flop reset inputs (see Figure 4). The flip-flop D inputs are fixed to 1. This topology ensures that only one or none of the flip-flops loads the D input per cycle, if the Rst signal arrives faster than the Clk_A and Clk_B signals to the flip-flops; that means the *Reset Path Delay* has to be shorter than the *Clock Path Delay* (RPD and CPD respectively in Figure 5). These different path delays ensure that the reset signal resets the flip-flops faster than the clock signal changes the flip-flop state, and also set the matching resolution between the phases of the filter output signal and the delayer output signal, as can be seen in the next section. The phase detector is the most delicate block in the auto-tuning system as it requires precise clock path delay stages between A_C and B_C and flip-flop clocks and resets.

C. *Phase Detector Block Deep review*

The phase detector must provide a pulse per cycle in C_d and no change in C_u when A is ahead, and a pulse per cycle in C_u and no pulse in C_d when B is ahead. To prevent undesired pulses, A_C to C_d delay (CPD) and B_C to C_u delay (same delay) must be longer than the via reset delay (B_C to C_d/C_u if A_C arrives first at the NAND gate). Furthermore, the system must not discriminate A to B lags shorter than a certain quantity if we want the system stabilizes at the best possible digital word.

Imagine A is ahead of B and let us call this lag ABD (see Figure 5). The A_C rise forces the flip-flop to load D value, which is fixed at 1, after CPD. This produces a rise in the C_d signal and the up/down counter counts down 1 (see Figure 4 and Figure 5). When the B_C rise occurs, it changes the NAND gate state causing activation of the flip-flop reset and the C_d signal to drop after the *Reset Path Delay* RPD=ND + RD. The pulse width generated in C_d is equal to ABD+RPD–

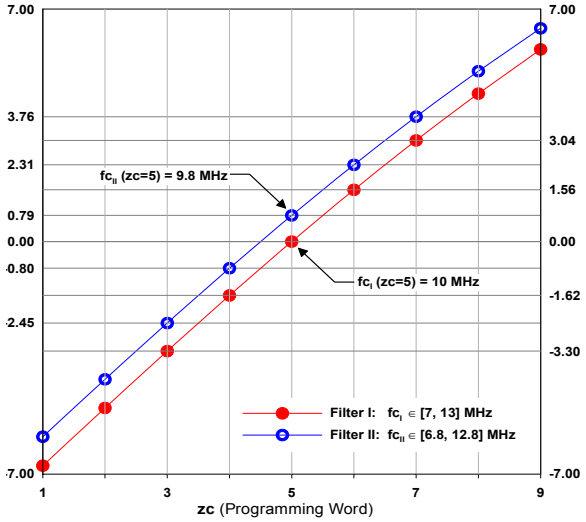

Figure 6. ABD versus programming word for two different tunable filters with Starting Cut-Off Frequency at 10 MHz and 9.8 MHz.

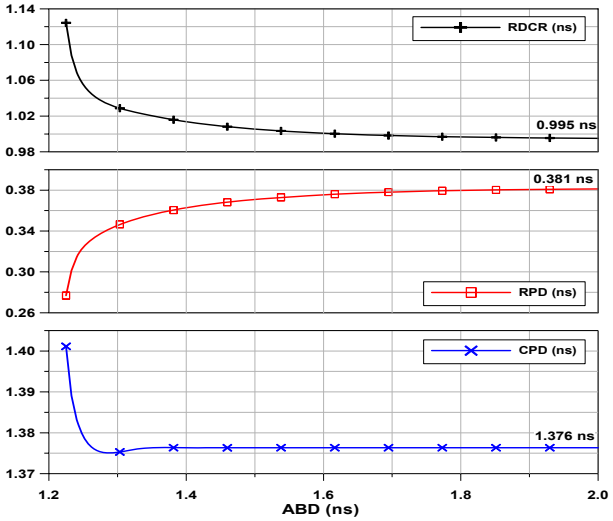

Figure 7. Delay study versus ABD lag.

CPD. When ABD ≤ CPD – RPD there is no pulse in C_d. As the lag from the B_c rise up to C_u rise is CPD too, the C_u state does not change and there is no pulse in C_d nor C_u.

The phase detector operation principle is based on achieving an accurate delay difference between the CPD lag and RPD lag. Because of the symmetry of the system with regard to the A_C and B_C signals the same occurs if B_C is ahead.

D. Delays restrictions Calculation

As shown in Section III C, a pulse is generated if the lag between A and B (ABD) is bigger than the Relative Delay between Clock path and Reset path, RDCR=CPD-RPD. The phase detector does not react for shorter values of ABD than RDCR, this quantity fixes the matching accuracy between the characteristic frequencies of the tuned system and the desired filter function. This lag must be calculated according to the desired characteristic frequency, tuning bit number and characteristic frequency accuracy attained at the integrated filter.

Two timing restrictions must be achieved. Firstly, the system must reach the best possible digital word ($\mathbf{zc}^{\infty}$) and secondly it must stabilize at this word without generating any pulse at either the C_u or the C_d outputs.

To achieve the second aim, the phase detector must not perceive shorter delays than ABD at $\mathbf{zc}^{\infty}$: ABD($\mathbf{zc}^{\infty}$). In this way, when the system arrives to this state there will not be any pulse at the phase detector outputs and the system remains stable at this state:

$$\text{RDCR} > \text{ABD}(\mathbf{zc}^{\infty}) \quad (1)$$

We will have the bigger ABD($\mathbf{zc}^{\infty}$) in a filter with the desired (nominal) characteristic frequency just in the middle of two consecutive programming words. A 10 MHz nominal cut-off frequency filter example of this situation is depicted in the Figure 6, where the fc_{II} plot represents a tunable filter with characteristic frequency at **zc** = 5 equals to 9.8 MHz and 10.2 MHz at **zc** = 4. As can be seen in this plot RDCR must be longer than 0.80 ns.

To ensure the system arrives to the best possible state the phase detector must detect any ABD lag longer than ABD($\mathbf{zc}^{\infty}$), then

$$\text{RDCR} < \text{ABD}(\mathbf{zc} \neq \mathbf{zc}^{\infty}) \quad (2)$$

The shortest ABD($\mathbf{zc} \neq \mathbf{zc}^{\infty}$) will be in a filter which matches the nominal characteristic frequency at one of the digital words. This is the case of the filter fc_I in Figure 6 where we can see that RDCR must be shorter than 1.56 ns.

In the Figure 6 example filter, the RDCR restrictions are:

$$0.80 \text{ ns} < \text{RDCR} < 1.56 \text{ ns} \quad (3)$$

Therefore, we can summarize that:

$$\text{ABD}(\mathbf{zc}^{\infty}) < \text{RDCR} < \text{ABD}(\mathbf{zc}), \text{ if } \mathbf{zc} \neq \mathbf{zc}^{\infty} \quad (4)$$

where $\mathbf{zc}^{\infty}$ is the programming word at the stable state.

IV. Phase Detector Viability Stydy: Simulation Results

Section III conclude the phase detector requires precise relative delay path implementation between reset and clock paths, RDCR. In our example, the phase detector RDCR must satisfy, 0.80 ns < RDCR < 1.56 ns to ensure the system stabilizes at the best digital word.

A good choice is 1.20 ns but this lag could change due to mismatching, ageing and working conditions. To ensure the viability of the system several simulations were carried out.

In Figure 4 each gate was implemented with the AMS c35b3 digital library [14]. The buffers were 7 library buffers (BUF2) in serial arrangement; this configuration provides a Clock Path Delay (CPD) of approximately 1.4 ns using library flip-flops (DFC1). The NAND gate was NAND20 and provides a Reset Path Delay (RPD) of 0.4 ns. Simulation results show this arrangement can detect delays between Ac and Bc (ABD) longer than 1.2 ns.

In Figure 7 RPD, CPD and RDCR dependences with ABD are presented. We can see this dependence is appreciable only when the relative (Ac, Bc) lag is shorter than 1.3 ns. At working frequencies this issue does not limit the tuning range (at any ABD value, RDCR < 1.20 ns) but to reach higher characteristic frequency filters, the implementation must be done using faster technologies with a shorter channel length.

Figure 8 represents tuneable filter parameters after the tuning process for 100 tuneable filters with Starting Cut-Off Frequency (frequency at **zc**=7) in the 6.8MHz–12.8MHz range. This interval represents a ±30% span from a nominal wanted 9.8MHz cut-off frequency, to consider potential changes in process and environment. Note that the final error is lower than 3%. The maximum tuning time was only 1.6 µs.

Figure 9 and TABLE I depict phase detector Monte Carlo analysis results. These analyses were carried out

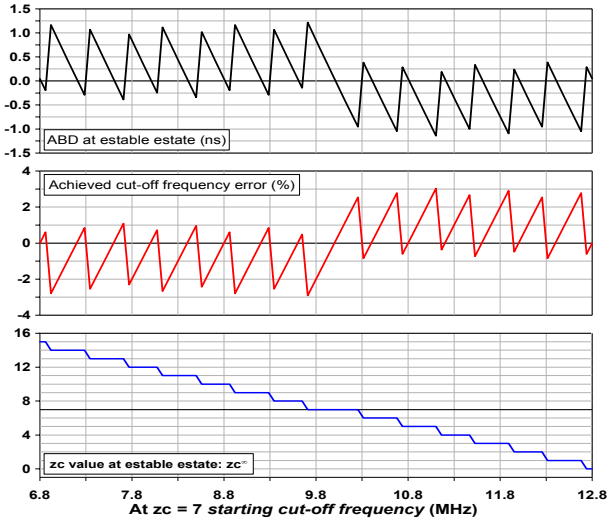

Figure 8. Final values for ABD, cut-off frequency error, and zc∞ after tuning process versus the Starting Cut-Off Frequency of a particular filter implementation.

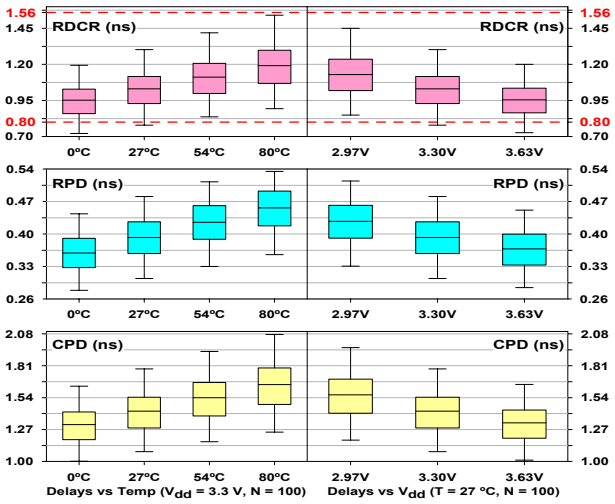

Figure 9. Phase detector delays 25%-box and MinMax-whisker plots versus temperature and bias voltage (Vdd). ABD=2ns.

without correlation definition for any element and taking into account both, mismatch and process alteration. Analysis results predict a RDCR compatible with the calculated values; consequently the building process will not significantly affect the phase detector resolution if a careful layout is developed.

V. Conclusions

A new auto-tuning technique for continuous-time filter is presented in this paper. Working principle is based on a phase detector with accurate relative path delays implementation. Preliminary studies show the phase detector building viability. The tuning scheme was shown on a Butterworth third-order low-pass filter yielding a 10 MHz cut-off frequency filter with an error lower than 3% and a tuning time of 1.6µs.

TABLE I. RDCR Monte Carlo analysis statistics.

ABD = 2 ns	RDCR(ns) T=27°C				RDCR(ns) Vdd=3.30 V		
	0°C	*27°C*	*54°C*	*80°C*	*2.97V*	*3.30V*	*3.63V*
Min.	0.72	0.78	0.84	0.89	0.85	0.78	0.73
Max.	1.19	1.30	1.42	1.54	1.45	1.30	1.20
Mean	0.95	1.03	1.11	1.19	1.13	1.03	0.96
1st quar.	0.86	0.93	1.00	1.07	1.02	0.93	0.87
3rd quar.	1.03	1.12	1.21	1.30	1.23	1.12	1.04
S.D.	0.11	0.12	0.13	0.15	0.13	0.12	0.11

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